HISTOGRAM TESTING OF ADC BY THE EXPONENTIAL SIGNAL

Roland HOLCER, Linus MICHAELI, Ján ŠALIGA
Department of Electronics and Multimedia Communications, Faculty of Electrical Engineering and Informatics,
Technical University of Košice, Letná 9, 042 00 Košice, tel. +421 55 602 2857,
E-mail: roland.holcer@tuke.sk, linus.michaeli@tuke.sk, jan.saliga@tuke.sk

SUMMARY

Testing of ADC's differential nonlinearity (DNL) by histogram method requires signal generator with extremely low distortion and high stability of the parameters. The new type of stimulus signal has been proposed, which achieves mentioned requirement. The studied testing signal has exponential form and is generated by discharging of the capacitor through known resistance. Besides precise signal shape the generating circuit could be ideally connected at the input of the ADC under test without interfering coupling with other instruments. The acquired digital samples from the output of ADC under test allow to determine the best fitted exponential signal by proposed three parametric method. The histogram from registered samples and that for the best fitted exponential shape allow to determine the differential nonlinearity DNL(k) for any code level k. In order to test each code level with similar number of samples the exponential shape was split into subparts. The acquired DNL(k) for each subranges are being fanfolded over the whole ADC input range. The proposed method has been experimentally verified for the ADC embedded on microcontroller ADuC812 where the testing results were compared by standardized methods.

Keywords: *ADC testing, histogram method, exponential stimulus signal*

1. INDRODUCTION

Differential and integral nonlinearity (DNL and INL) of the Analogue to Digital Converter (ADC) are functional parameters, which describes deviation of actual A/D transfer characteristic from the ideal one. A dynamic testing method using histogram assess the distribution of the acquired samples for known stimulus signal, carrying information about actual $DNL(k)$ of ADC under test. Well known feature of this approach is reduced testing time compared with static methods. On the other hand, the high accuracy of stimulus signal generator, comparable with accuracy of a DC calibrator is the dominant weakness of the dynamic testing in statistical domain. Various approaches have been proposed in the literature [3], [4], [5] which allow to overcome the mentioned problem. Interfering input voltages of various origin and thermal noise tend to equalize the code bin width $W(k)$ in the ADC under test and hides $DNL(k)$ errors in the histogram shape. The only parameter which displays this undesirable "dithering effect" is effective number of bits which is coming down in spite of improving value of the differential nonlinearity. For the mentioned reasons the testing stand besides high accuracy of the stimulus signal shape requires extremely high reduction of the electromagnetic interference generated on the ground wires. This covering effect uplifts the testing results in comparison with the real $DNL(k)$ values.

Reduction of the interfering and noise voltages generated over the impedances of the ground wires could be achieved easily by the generator powered independently from ADC under test and other instruments installed at the testing stand. The star-like connection of the grounds is the necessary condition for optimal suppression of the interfering sources.

The classical histogram test method utilizes harmonic test signal with extremely low distortion as the source of testing signal. Implementation of band-pass linear filter with high quality allows to reduce spectral impurities caused by non-linearity of testing generator and noise of the output amplifier. The optimal calibrating voltage is that, which is supplied from proper electrochemical source and connected star-like at the ground terminal of the ADC input. The histogram testing method requires testing voltage to be time dependent and exactly determined.

The new method of testing signal generation is described in the paper, represented by the voltage of discharged capacity through known resistance. The advantages of such signal are represented by closeness of real signal shape to the ideal one and the easy circuit implementation which is ideally decoupled from the common supply source. The acquired digital samples from the output of ADC under test allow to assess best fitted exponential shape. The histogram obtained from this flux allows to estimate the real code bin width $W(k)$ and the differential nonlinearity $DNL(k)$ for any code level.

2. GENERATION OF STIMULUS VOLTAGE

Generator of the stimulus signal connected to the ADC is shown in Fig. 1. Testing voltage is generated by the parallel RC circuit disconnected from the independent supply voltage U_{ST} by a magnetic relay. After switching off, the capacitor C is discharged by the resistance R in parallel with the ADC input resistance R_{IN}. The input current I_{IN} of the ADC generates on the input resistance R_{IN} offset voltage U_{off}. The offset voltage represents the bias value of the stimulus signal. The initial glitches of the exponential shape caused by the magnetic relay are avoided by the shifted origin of the accumulated

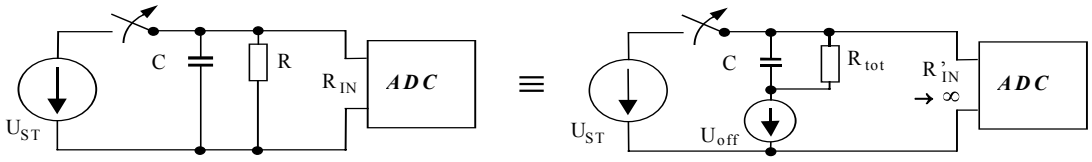

Fig. 1a Circuit generating exponential stimulus signal

Fig. 1b Equivalent circuit

samples from the output data flux, just after the end of transition process. The caused time jitter does not impact the shape of the best fitted exponential shape. The equivalent circuit is shown in Fig. 1b.

The differential nonlinearity of ADC under test is estimated from the histogram of registered samples using well known formula

$$DNL(k) = \frac{P_{act}(k)}{P_{id}(k)} - 1 \quad \text{[LSB]} \tag{1}$$

where $P_{id}(k)$ is the number of occurrences of each k for ideally exponential shape of stimulus signal. $P_{act}(k)$ represents the actual number of output codes with the digital value equal to k. Ideal shape of the discharging calibration voltage is

$$U_{\mathrm{IN}} = U_{\mathrm{off}} + (\mathrm{U_{ST}} - U_{\mathrm{off}})\mathrm{e}^{-\frac{t}{RC}} \tag{2}$$

The ideal value of occurrence of output samples $P_{id}(k)$ with code bin k has been determined for exponentially shaped stimulus by

$$P_{id}(k) = -RCf_S \ln\left(\frac{kQ - U_{off}}{(k+1)Q - U_{off}}\right) \tag{3}$$
$$for \quad k = \left(2^N - 2\right),..,1;$$

where U_{ST}, and U_{off} are known from the Fig. 1b. Sampling frequency is f_S. The Q is ideal code bin width defined according to [2].

The ideal shape of the stimulus signal is unknown. The standardized methods utilize three or four parameters fitting algorithm for the estimation of testing harmonic signal parameters [1], [2]. Similarly, the parameters of the exponential input signal could be identified by the three parametric fitting procedure from the acquired data flux modified for this particularity.

Let us consider a data flux of M time samples registered in the vector form $Y=[y(1),y(2),..y(M)]^{\mathrm{T}}$. The criterial function for least square method, which has to be minimized, is

$$\frac{1}{M}\sum_{m=1}^{M}\left[y(m) - A - Be^{mH}\right]^2 = \varepsilon^2(A,B,H) \tag{4}$$

Moreover the value ε^2 contains the quantization noise power. Three parameters A, B, H characterize the optimal estimate of stimulus signal at the input of ADC. The constant H is the inverted time constant normalized to the actual value of the sampling frequency. Optimization procedure is based on minimization of partial derivations $\partial\varepsilon^2/\partial A, \partial\varepsilon^2/\partial B, \partial\varepsilon^2/\partial H$ according of the optimized constants A, B, H. The determination of the parameters A,B,H could be performed iteratively. Normalised exponential shape for i-th estimate of the inverted time constant $H(i)$ is represented by matrix $D(i)$. I-th estimate of the coefficients $A(i)$ and $B(i)$ is represented by the vector $X(i)$. The input data flux is described by vector Y.

$$\mathbf{D}(i) = \begin{bmatrix} 1 & \mathrm{e}^{H(i)} \\ 1 & \mathrm{e}^{2H(i)} \\ \vdots & \vdots \\ 1 & \mathrm{e}^{MH(i)} \end{bmatrix}; \quad \mathbf{X}(i) = \begin{bmatrix} A(i) \\ B(i) \end{bmatrix}; \quad \mathbf{Y} = \begin{bmatrix} y(1) \\ y(2) \\ \vdots \\ y(M) \end{bmatrix} \tag{5}$$

The criterial function (4) in the i-th iteration step expressed in the matrix form is

$$\frac{1}{M}\sum_{m=1}^{M}\left[y(m) - A(i) - B(i)e^{mH(i)}\right]^2 = \frac{1}{M}\left(\mathbf{Y}\text{-}\mathbf{D}(i)\mathbf{X}(i)\right)^{\mathrm{T}}\left(\mathbf{Y}\text{-}\mathbf{D}(i)\mathbf{X}(i)\right) = \varepsilon^2 \tag{6}$$

The proposed iteration algorithm is similar to that utilized in the four parametric estimation of the harmonic function parameters [1], [2]. The initial assessment of the coefficients $X(1)=[A(1),B(1)]^{\mathrm{T}}$ is obtained in the first iteration step using the theoretically expected value $H(1)$. The i-th iterate of the coefficients in vector $X(i)$ are calculated for the minimum of the squared differences ε^2.

$$\mathbf{X}(i) = \left(\mathbf{D}(i)^{\mathrm{T}}\,\mathbf{D}(i)\right)^{-1}\left(\mathbf{D}(i)^{\mathrm{T}}\,\mathbf{Y}\right) \tag{7}$$

The coefficient $H(i)$ in the vector $D(i)$ for the next iteration is chosen by gradient optimization algorithm with aim to minimize ε^2. The procedure is finished after I-th iteration when $|\varepsilon^2(I) - \varepsilon^2(I\text{-}1)| \le 0.01$.

The approximated shape allow to determine ideal occurrences for the condition of the k-th ideal code bin width equal to $W_{id}(k) = Q$.

$$P_{id}(k) = \frac{M}{H(I)}\ln\left(\frac{k - A(I)}{k - 1 - A(I)}\right) \tag{8}$$

The final calculus of $DNL(k)$ is calculated from (1).

Exponential stimulus signal is characterized by the same drawback as harmonic one caused by the different occurrence of output samples for each code level k. The equality of the code bin k occurrence is being achieved when the duration of the input voltage across every code bin width $W(k)$ will be similar. This goal is being achieved by the splitting of the ADC full range into some subparts, Fig. 2.

The partial subrange is tested by the stimulus signal with different time constant RC. The sequences of output data are banded in such manner that the adjacent code bin ranges are tested by two stimulus signals with two time constants. They will be chosen in such a way to have approximately identical duration of stimulus signal in the range of every code bin width. Advantage of such method is proportionality of the uncertainty in the histogram measurement and less demand on the total number of samples M required for obtaining sufficiently high occurrence with the investigated code value k.

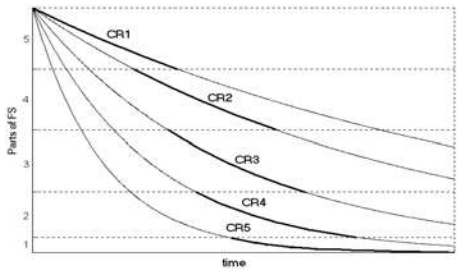

Fig. 2 Dividing of the full-scale range into more parts

3. EXPERIMENTAL RESULTS

The proposed method has been experimentally verified for the ADC embedded on microcontroller ADuC812 [7] where the testing results were compared by standardized methods. Fig. 3 shows the generated subparts and calculated shapes of $DNL(k)$ by (1). Every subpart has been identified by the proposed fitting method. Testing stand with generator circuit is shown in Fig. 4.

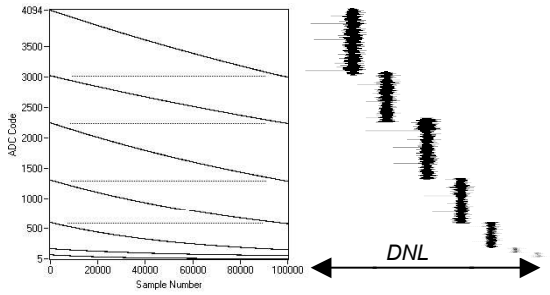

Fig. 3 Generated exponential subparts and measured $DNL(k)$ from the histogram of output data record

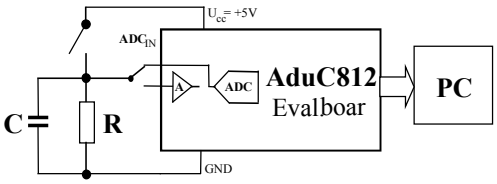

Fig. 4 Setup for exponential wave testing in position without buffering amplifier

Buffering amplifier on the front end causes additional nonlinearity and disables testing occurrences of some first codes near to ground. For these reasons, the buffering amplifier was disconnected and testing signal was applied directly to ADC input. The discharging resistances for single subparts for $M=10^5$ samples are presented in Tab. 1.

Number of samples M = 100000	
V_{ST}=2,5V	
Without buffering amplifier	
C=9.3μF	
Codes	R[Ω]
4094-2994	∞
3020-2237	∞
2250-1292	3M9
1310-577	1M8
600-152	820k
172-59	680k
70-5	390k

Tab. 1 Resistances in the discharging circuit

The measured $DNL(k)$ subranges for each exponential subpart has been seamed into the final shape for all input voltage ranges. Experiments were performed for exponentially shaped signals without input buffering amplifier, Fig. 5a). Their counterpart Fig. 5b) is the shape of the integral nonlinearity calculated by integration formula:

$$INL(k) = \sum_{j=1}^{k} DNL(j) \qquad \text{[LSB]} \tag{9}$$

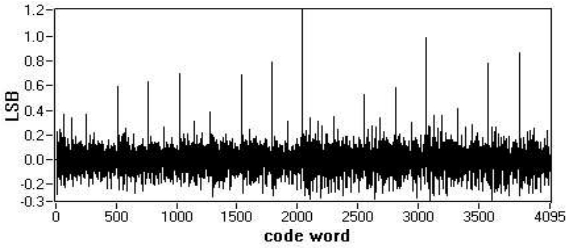

Fig. 5a Differential nonlinearity of ADuC812 by exponential testing

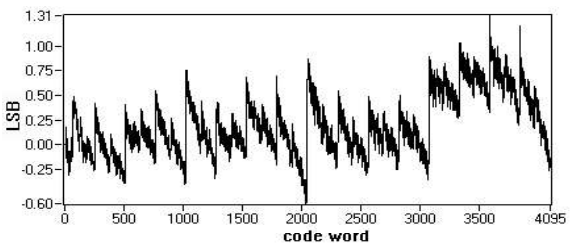

Fig. 5b Integral nonlinearity of ADuC812 by exponential testing

The obtained results were compared with the testing results using standardized histogram method [2] by harmonic stimulus signal (Fig. 6).

From this reference ADC testing the results of DNL measured by the proposed and standardized method are similar. The calculated *INL*(*k*) accumulates testing uncertainty and the distortion of input amplifier and it shows the contribution of an additional circuit to the total nonlinearity of stimulus signal generator.

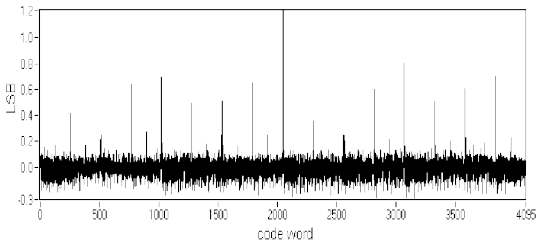

Fig. 6a Differential nonlinearity of ADuC812 obtained by the standardized histogram test

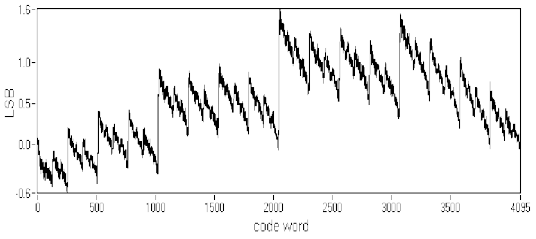

Fig. 6b Integral nonlinearity of ADuC812 calculated from the *DNL*(*k*) tested by the standardized histogram

4. CONCLUSION

The authors proposed the new and simple histogram method for dynamic testing of ADC differential nonlinearity based on exponential stimulus signal. Because of low slope of the testing signals, the measured differential nonlinearity is close to the values estimated by the static testing method. Proposed exponential testing signal is easy to generate with required accuracy. Moreover the circuit generating such stimulus signal is ideally decoupled from any interfering sources and control computer at the testing stand. The idealized test signal is approximated from the ADC output flux by best fitted exponential function. The fitting algorithm is iterative, similar to the known four - parameter estimation of best fitted harmonic function. The comparison of the proposed testing method with standardized histogram method for harmonic stimulus signal shoved good coherence. The proposed testing approach has good traceability with the standardized static testing method or quasi-static histogram testing method with low-frequency harmonic testing signal. The bottleneck of the proposed method is the situation represented by low input voltage, where high values of capacities are required. Authors are solving this disadvantage using coherent acquisition of periodic exponential shape generated by electronically switched RC circuit. The dielectric absorption of discharging capacitor could distort the expected exponential stimulus signal shape. Increasing number of assessed samples allows to reduce the confidential interval for estimation of measured histogram. Because of low voltage slope, the proposed histogram test is being close to the static testing method.

REFERENCES

[1] IEEE Std. 1057 - 1994, "IEEE Standard for Digitizing Waveform Recorders," Institute of Electrical and Electronics Engineers, Inc., New York, USA, 1994

[2] IEEE Std. 1241 - 2000, "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," Institute of Electrical and Electronics Engineers, Inc. New York, USA, 2000

[3] Belcher, R. A.: "Multi-tone testing of quantisers using PRBS signal," Computer standards & interfaces, Vol. 22, Number 4, October 2000, pp.269-279.

[4] Pokorný, M., Roztočil, J., Haasz, V.: "Suppression of Test Signal Distortion by A/D Modules Dynamic Testing," IMEKO TC4 Symposium on Development in Digital Measuring Instrumentation, Naples, September 1998.

[5] Alegria, F. Arpaia, P. Daponte, P. Cruz Serra, A.: "ADC Histogram Test Using Small Amplitude Input Waves," Proceedings of XVI IMEKO World Congress, Vienna, Austria, 2000, Sept.25-28. Vol. X, EWADC' 2000, pp.33-38.

[6] Michaeli, L.: "A fast method for correction of systematic errors of ADC in histogram measurements," Proceedings of IMEKO 10th Int. Congress, Prague, Vol. 2, pp. 40-47, 1985.

[7] Holcer, R.: "The Performance Test of the AD Converters Embedded On Some Microcontrollers," Proceedings of XVI IMEKO World Congress, Vienna, Austria, 2000, Sept. 25-28. Vol. X, EWADC'2000, pp. 165-169.

[8] Matyáš, V.: "Měření, analýza a vytváření náhodních procesu," SNTL, Praha, 1976.

BIOGRAPHY

Roland Holcer was born in Košice, Slovak Republic, in 1976. He received Ing. degree in Electrical Engineering in 1999 from the Dept. of Electronics and Telecommunications, on Technical University of Košice. Since 2000 he is an internal PhD student on the same department in the field of ADC testing.

Linus Michaeli was born in Žilina, Slovak Republik in 1945. He received Ing. degree in Telecommunications from the Technical University of Transport in 1968 and PhD degree at the Slovak Technical University of Bratislava in 1979. Since 1994 he is full professor at the Dept. of electronics and multimedial telecommunications, Technical University of Košice. He is the Slovak member of the IMEKO TC4. His main research interests are in ADC modeling and testing and artificial neural network for measurement signal processing.

Ján Šaliga was born in 1958. He received Ing. degree in Electrical Engineering in 1982 and his PhD in Radioelectronics in 1995 from the Technical University in Košice. Since 1984 he was assistant professor at Technical University in Košice, Department of Electronics and Multimedial Telecommunication. Now, he is associated professor at this. His present research activities are focused on ADC and DAC testing methodology, general measurement methods, virtual instrumentation and distributed measurement systems.