SIMULATION OF HEAT TRANSFER BY COOLING CHANNELS IN LTCC SUBSTRATE

Tomas GIRASEK*, Alena PIETRIKOVA*, Tilo WELKER**, Jens MÜLLER**
*Department of Technologies in Electronics, Faculty of Electrical Engineering and Informatics,
Technical University of Košice, Letná 9, 042 00 Košice, Slovak Republic, Tel.: +421 55 602 3014, E-mail: tomas.girasek@tuke.sk
**Electronics Technology Group, Technical University of Ilmenau, Gustav-Kirchhoff-Str.1, Ilmenau, 98693, Germany

ABSTRACT

The thermal resistance, flow analysis, pressure drop and distribution of coolant inside multilayer LTCC (Low Temperature Co-fired Ceramics) substrate are detailed investigated in this paper. For this reason four various structures of internal channels in the multilayer LTCC substrates were designed and simulated. The simulation 3D model consist of 6 LTCC of DuPont 951® layer with cooling microchannel in middle of substrate, power chips paced on top of LTCC and silver sintered joints under power chips. The impact of the structure of channels, volume flow and power loss of die was simulated, calculated and analyzed by using the simulation software Mentor Graphics FloEFD™. The structure and size of channels have the significant impact on thermal resistance, pressure of coolant as well as the effectivity of cooling power components which can be placed on LTCC substrate. The thermal resistance was calculated from the temperature gradient among chip junction, the inlet fluid and the thermal load of chip. Optimizing and comparison of cooling channels structure inside LTCC substrates and analyzing the effect of volume flow for achieving the least thermal resistance of LTCC multilayer substrate is the main contribution of this paper.

Keywords: *thermal simulation, thermal resistance, LTCC, cooling channels*

1. INTRODUCTION

Nowadays is thermal management of electronic devices serious problem because of electronics miniaturization, high performance and high reliability. The amount of the heat flux is growing up by the improvement of chip integration, package density, small size, layer quality, high frequency and high power loss in small area [1, 2]. The electronic devices used in power electronic applications have to work properly in a very wide temperature range up to 200°C. High temperature changes generate large thermal stress that affects power devices reliability. Therefore the thermal analysis has been carried out at the preliminary stage of the manufacturing and design.

LTCC technology with embedded microchannel is novel application in automotive technology, avionics, biology, military and telecommunication applications where the heat dissipation and high frequency property are mainly required [3, 4, 9]. In the recent years the interest of the fluidic structures in LTCC is growing [2, 5, 9]. LTCC is well suited as package solution for harsh environments due to their inherent features such as excellent thermal and chemical stability, hermeticity, simple 3D structuration, matching of thermal expansion coefficient with silicon and possibility of different fluidic and electrical component integration inside one ceramic substrate [3, 10, 11]. These interesting features can be used in different applications of industry, where is the necessity to cooling the devices by the coolant inside the microfluidic system [1, 2, 4, 5, 7, 9].

LTCC technology via small channels allows a promising solution for improving heat dissipation and for decreasing the limited high temperature from the power chip. However, the poor thermal conductivity (which is about 3 to 5 $Wm^{-1}K^{-1}$) limits their application for power electronic [5, 6]. For this reason the poor thermal conductivity of LTCC has to be improved by a coolant, which is pumped through the fluidic channels inside the LTCC devices [1, 3, 4, 6, 7, 8]. Integrated microchannel cooling system in LTCC substrate can decrease the additional temperature more than 80 % [20]. The main advantage of LTCC substrate with integrated liquid cooling system is the heat dissipation from the point of the thermal source. For this reason these devices provide an excellent thermal performance for high power application with theoretical heat flux of 1000 $W.cm^{-2}$ [1, 4]. Moreover the LTCC devices may not be bonded to a metal heat sink, which reduces material, weight and volume that means less process' steps within production.

This paper presents the comparison of thermal resistance, flow analysis and distribution of coolant in four various structures of internal channels in multilayer LTCC substrates. The dimensions and structure of microchannel has been chosen and modified to obtain better cooling performance for different working conditions. The heat transfer behaviors was characterized by the decrease of maximum working temperature, thermal resistance of substrate, temperature distribution, fluid pressure and flow velocity fields. Presented designs ware simulated by using the simulation software Mentor Graphic FloEFD™.

The main motivation for creation of this work was analysis and calculation of heat transfer, impact of channels' shape to pressure drop that is expressed by particular numerical results oriented to reducing the thermal resistance. Moreover in power applications is necessary to know the impact of the thermal load of first chip on the temperature of the second chip. The presented results will be helpful for the optimization of design the cooling microchannel structure in future work with the real multilayer structures for high power devices.

2. INTERNAL CHANNELS STRUCTURE

The used material for the experiments was a commercially available LTCC green tape DuPont 951® with thermal conductivity 3.3 $Wm^{-1}K^{-1}$. The created 3D model consists of 6 layers of DuPont 951® with 0.214 mm

thickness and SiC chip with thermal conductivity 120 $Wm^{-1}K^{-1}$ and dimension 10 x 10 x 1 mm^3 such as the thermal load generator. Thickness of the LTCC substrate was 1.2 mm. The fluidic channel integrated in the third layer from the top of the 3D model has the cross sectional area of 2 x 0.214 mm^2 for the shape #1, #2, #3 and 10 x 0.214 mm^2 for the shape #4. All dimensions of the structures are listed in the Table 1. Multilayer structure of LTCC substrate is shown in the Fig. 1.

Table 1 Structures dimensions

Structures	#1	#2	#3	#4
Width of channel [mm]	2	2	2	10
Length of channel [mm]	105	150	3 x 48	48
Thickness of channel [mm]	0.214	0.214	0.214	0.214
Area under the chip [mm^2]	71	60	60	100
Inlet hole dimension [mm]	2	2	2	2
Outlet hole dimension [mm]	2	2	2	2

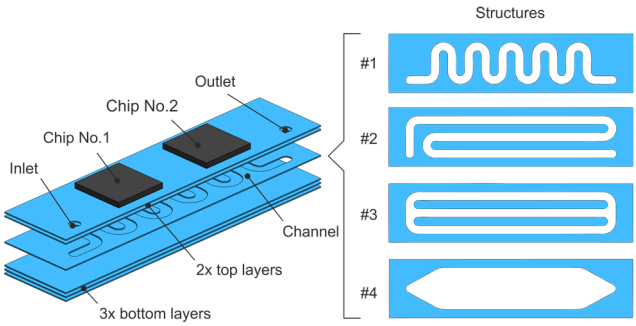

Fig. 1 Multilayer structure of LTCC substrate with microchannels

Between the power chips and LTCC substrate is the layer of silver pads and the layer of silver sintered joint. The dimension of both layers is 10 x 10 mm^2 and the thickness is 10 µm. Thermal conductivity of silver sintered joints are 140 $W.m^{-1}K^{-1}$ and for silver pads are 360 $W.m^{-1}K^{-1}$. The silver sintered joints was used for they high thermal stability and high thermal conductivity. In all structure is used one channel of LTCC layer with thickness 0.214 mm. Inlet and outlet holes are the same for every substrate and diameter of holes are 2 mm. The position of power chip on the substrate was selected due to need to cooling the largest area of the chip by the flow of coolant in the channels. For the investigation of the impact of the first chips' thermal load on the second chip, two chips placed on LTCC substrate were used. Fig. 2 illustrates the cross section of the structure #4 of the cooling concepts realized by LTCC technology.

3. SIMULATIONS

The thermal performance of analyzed cooling methods was evaluated by the simulations in Mentor Graphics FloEFD™ commercial simulation software. The junction temperature of the chip was simulated for a constant volume flow of coolant through the fluidic channels. For the simulation of the coolant the demineralized water with an inlet temperature of 20°C was used. The thermal load of the chip was selected by the maximum junction temperature which does not exceed the boiling point of the water. The thermal resistance (R_{th}) was calculated from the temperature gradient among chip junction (υ_j), the inlet fluid (υ_{if}) and the thermal load (P) of chip (1) [5].

$$R_{th} = \frac{\vartheta_j - \vartheta_{if}}{P} \; [K.W^{-1}] \qquad (1)$$

The thermal resistance was calculated for different volume flow rate with the range of 10 $ml.min^{-1}$ to 300 $ml.min^{-1}$.

The first type of channel (#1) was designed with 11 curves in the shape of meander. This channel was chose for simulation and investigation of the curves' impact on the fluid's pressure inside the channels. The cooling area under one power chip in the structure #1 is 71 mm^2. The difference between the structures #1 and #2 is in the number of used curves which can reduce the pressure in the channel with maintaining the effectiveness of cooling. Cooling area under one of power chip in this structure is 60 mm^2.

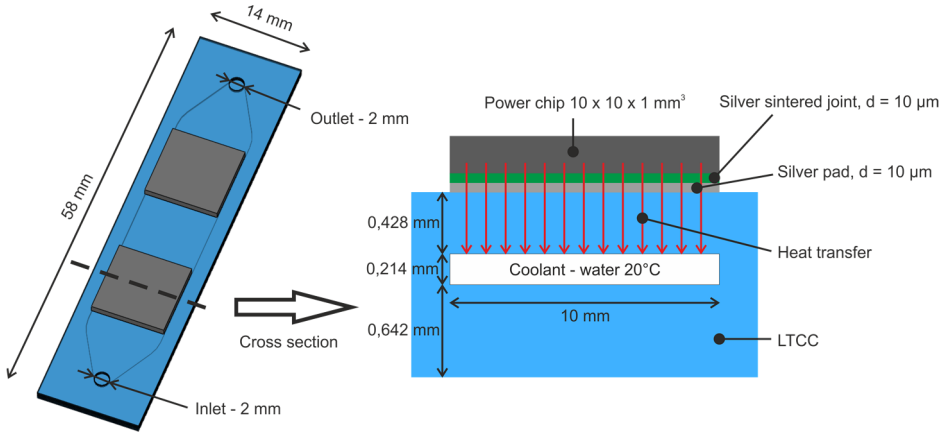

Fig. 2 Cross section of the simulation model with structure #4

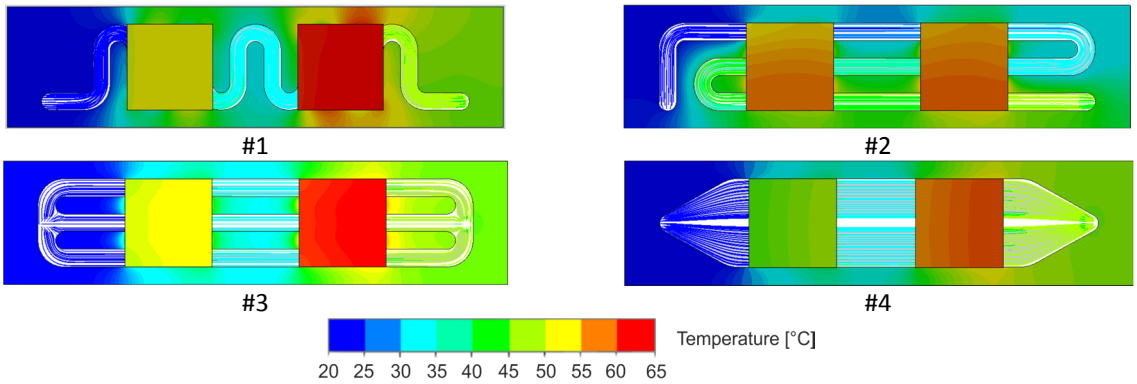

Fig. 3 Simulated temperature distribution of structure #1, #2, #3 and #4 at the thermal load of 10W per chip. The volume flow is set to 10 ml.min-1 and coolant fluid from left side to right.

The structure #3 has three separate channels with a few curves such as can be seen in the Fig. 1. This structure of channel was created for the minimization of the pressure during high flow rate of water. The cooling area under the power chip is 60 mm^2. The last structure #4 has the one big channel with largest area of 100 mm^2. However, the big cross section of channel provides fluently flow rate with minimum turbulence and decrease the pressure inside channel. Fig. 3 shows the simulated temperature distribution by coolant and substrate from the power chips realized by Mentor Graphics FloEFD™. It can be seen that the temperature distribution was from the left side (inlet) to right side (outlet), what was caused by fluidic coolant. The volume flow rate of coolant was set to 10 ml.min^{-1}. The simulations demonstrate the impact of the thermal load of first chip (left) on temperature of the second chip (right). The minimum impact is in the case of structure #2, which can be seen in the Fig. 3 as well as in the Fig. 5.

4. RESULTS OF SIMULATIONS AND DISCUSSION

In the Fig. 4 the thermal resistance as a function of the volume flow rate of all 4 structures is plotted. The simulations demonstrate the design #4 had the lowest thermal resistance. The biggest channel inside LTCC substrate reduces the thermal resistance by 2.8 % in average. The structure #2 had the worst thermal resistivity in the case of the flow rate was less than 50 ml.min^{-1}. It can be seen that the thermal resistance is significantly dependent on the volume flow rate. At volume flow rate lower than 50 ml.min^{-1} the thermal resistance (R_{th}) increases exponentially. On the other hand, the thermal resistance above 50 ml.min^{-1} decreases slowly as it can be seen in the Fig. 4.

The pressure of coolant inside the channel is also dependent on the volume flow rate which is shown in the Fig. 4. The highest pressure (13.4 bar at 300 ml.min^{-1}) was in the case of structure #1. In the structures #1 and #2 the pressure increases significantly by increasing the flow rate. The lowest pressure 1.2 bar in average had the structure #3 and #4. These structures have almost constant pressure during all volume of flow rate.

Structure #4 is the most promising candidate to cooling power chips on LTCC substrate for the reason of low thermal resistance at different volume flow rate as well as the simple fabrication requirements. In this structure the optimal flow rate to cooling the power chip is 150 ml.min^{-1}. If the volume flow rate increases above 150 ml.min^{-1} the thermal resistance is relatively stable (Fig. 4). Structure #4 gives possibility for optimal flow rate and optimal cooling effect of power chips.

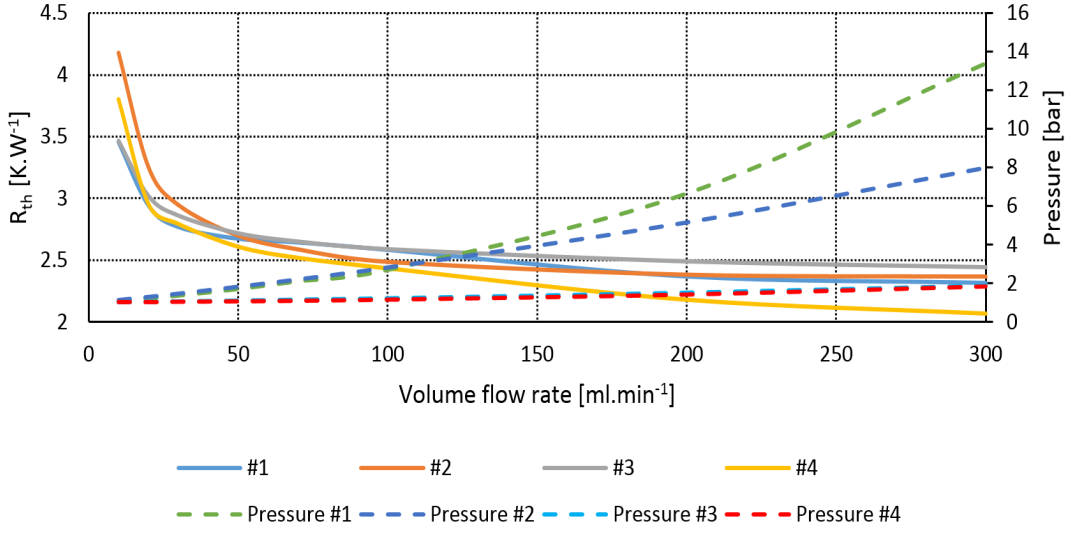

Fig. 4 The influence of volume flow rate on the thermal resistance and pressure

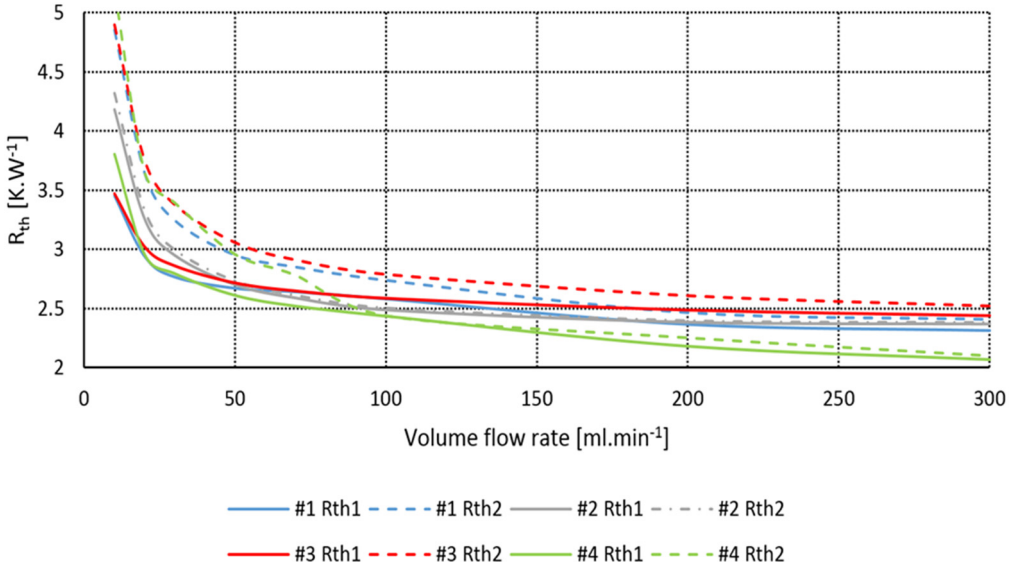

Fig. 5 The influence of volume flow rate on the thermal resistance and pressure

In the Fig. 5 the thermal resistance of both chips as a function of the volume flow rate is plotted. The simulations demonstrate the impact of the thermal load of the first chip (No. 1) on the temperature of the second chip (No. 2). The thermal resistance of substrate was different for the chips No. 1 and No. 2 in all structures. The highest difference of thermal resistance is at structure #1, #3 and #4, 16 % in average. This difference was caused by direct flow of fluid from chip No. 1 to chip No. 2. At the chip No. 1 there was the transfer of the thermal energy on to chip No. 2 by the coolant in the channel. At the structure #4 the difference of the thermal resistance is approximately 4 % at optimal flow rate 150 ml.min^{-1}. The minimum difference of 1.3 % is at the structure #2. It is because the coolant flows from the chip No. 1 to chip No. 2 in the first step. After this the coolant continues again to the chip No. 1, which causes the balanced thermal resistance of both chips (Fig. 3).

5. CONCLUSIONS

The LTCC substrates with fluidic channels simulated by a Mentor Graphics FloEFD^{TM} was presented in this paper. The influence of the channel structures on the thermal resistance and pressure of the coolant was investigated. The simulations show there is a nonlinear relation between the volume flow rate and the thermal resistance. Increasing the mass flow rate of the coolant causes the reduction of the thermal conductivity as well as causes the pressure rise inside the channels. The structures of channels have the significant impact on the coolant pressure. Substrate with structure #4 is the most promising candidate to cooling power chips on LTCC substrate, for the reason of low thermal resistance at different volume flow rate. Structure #4 reduces the thermal resistance by 2.8 % in average by contrast to structure #1, #2 and #3. LTCC structure with embedded microchannel structure #4 decrease additional temperature of chips about 86 % (at 2 W) in average by contrast to LTCC substrate without cooling channels. Volume rate flow at the structure #4 at the power loss of 10 W was from 10 ml.min^{-1} to 300 ml.min^{-1}. Thermal resistance continuously decreases at this volume flow rate from 3.8 K.W^{-1} to 2.06 K.W^{-1}. The structure of microchannel #3 characterized in that thermal resistance at the flow rate from 50 ml.min^{-1} to 300 ml.min^{-1} was nearly invariable. The structure of microchannel #3 represents the less effective cooler.

The simulations demonstrate the impact of the thermal load of first chip (No. 1) on the temperature of the second chip (No. 2) as well as. The minimum difference 1.3 % of the thermal resistance was at structure #2. At the other structures the difference of the thermal resistance was approximately 12.9 % in average at the volume rate flow lower than 150 ml.min^{-1}.

Multilayer structure of LTCC substrate with microchannel represents new modern and effective approach to cooling systems in power electronics. The importance of this new technology is very significant in continuous miniaturisation of power modules.

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BIOGRAPHIES

Tomas Girasek was born on 1989. In 2014 he graduated (MSc) with distinction at the Department of Technologies in Electronics of the Faculty of Electrical Engineering and Informatics at Technical University of Košice. Now, he is a PhD. student at the same department. His scientific research is oriented to thermal management, multilayer structures, ceramic circuits and joints in power electronics.

Alena Pietrikova is full professor (2007) of Electrotechnology and Materials at the Faculty of Electrical Engineering and Informatics Technical University of Košice, Slovak Republic. Her research work is concentrated on problems concerned with modern materials and technologies in electronics (film technologies, assembling technologies in electronics, and materials for electronics). She is an author or co-author of more than 250 research articles in international journals or conference proceedings, 5 patents and 5 books.

Tilo Welker, born in 1984, received his Diploma degree in computer engineering specialized in integrated hard- and software systems 2009, from the Ilmenau University of Technology, Germany. He is a scientific coworker at the Institute of Micro- and Nanotechnologies at the Ilmenau University of Technology, Germany. Main interest of his research include thermal management, packaging, ceramic circuits and 3D integration.

Jens Müller, born September 1965, received his diploma degree for electrical engineering and the doctoral degree from Ilmenau University of Technology, Ilmenau, Germany, in 1992 and 1997 respectively. In July 2008 he was assigned full professor for the Department of Electronics Technology at the same university. His particular research interest covers functional integration for ceramic based System-in-Packages considering aspects of harsh environmental use, and high thermal / high-frequency requirements with a strong focus on LTCC materials and its combination with Silicon by a proprietary process.